CLAIMS:

What is claimed is:

1. A method in a multi-processor data processing system for changing an operating frequency for a system core logic used to interface to memory in the multi-processor data processing system, the method comprising:

determining whether the operating frequency should be changed from a default frequency to another frequency;

responsive to determining the operating frequency should be changed from the default frequency to the another frequency, placing slave processors in the multi-processor data processing system into a non-transactional mode; and

changing the operating frequency in the system core logic to the another frequency.

2. The method of claim 1 further comprising:

placing the slave processors into a normal mode.

3. The method of claim 2 further comprising:

completing initialization of the multi processor data processing system.

4. The method of claim 1, wherein the non-transactional mode is a sleep mode.

5. The method of claim 1, wherein the non-transactional mode is a mode in which the slave processors are in a spin loop without generating any external bus transactions.

6. The method of claim 1, wherein the changing step comprises:

setting a register in the system core logic to a value for the another frequency.

7. The method of claim 1, wherein the determining step, the placing step, and the changing step are performed by a master processor in the multi-processor data processing system.

8. The method of claim 1, wherein the multi-processor data processing system is a symmetric multi-processor data processing system.

9. A multi-processor data processing system for changing an operating frequency for a system core logic used to interface to memory in the multi-processor data processing system, the multi-processor data processing system comprising:

determining means for determining whether the operating frequency should be changed from the default frequency to the another frequency;

placing means, responsive to determining the operating frequency should be changed from a default frequency to another frequency, for placing slave

processors in the multi-processor data processing system into a non-transactional mode; and

changing means for changing the operating frequency in the system core logic to the another frequency.

10. The multi-processor data processing system of claim 9, wherein the placing means is the first placing means and further comprising:

second placing means for placing the slave processors into a normal mode.

11. The multi-processor data processing system of claim 10 further comprising:

completing means for completing initialization of the multi processor data processing system.

12. The multi-processor data processing system of claim 9, wherein the non-transactional mode is a sleep mode.

13. The multi-processor data processing system of claim 9, wherein the non-transactional mode is a mode in which the slave processors are in a spin loop without generating any external bus transactions.

14. The multi-processor data processing system of claim 9, wherein the changing means comprises:

setting means for setting a register in the system core logic to a value for the another frequency.

15. The multi-processor data processing system of claim 9, wherein the determining means, the placing means, and the changing means are located in a master processor in the multi-processor data processing system.

16. The multi-processor data processing system of claim 9, wherein the multi-processor data processing system is a symmetric multi-processor data processing system.

17. A computer program product in a computer readable medium for changing an operating frequency for a system core logic used to interface to memory in a multi-processor data processing system, the computer program product comprising:

first instructions for determining whether the operating frequency should be changed from the default frequency to the another frequency;

second instructions, responsive to determining the operating frequency should be changed from a default frequency to another frequency, for placing slave processors in the multi-processor data processing system into a non-transactional mode; and

third instructions for changing the operating frequency in the system core logic to the another frequency.

18. The computer program product of claim 17 further comprising:

fourth instructions for placing the slave processors into a normal mode.

19. The computer program product of claim 18 further comprising:

fifth instructions for completing initialization of the multi processor data processing system.

20. The computer program product of claim 17, wherein the non-transactional mode is a sleep mode.

21. The computer program product of claim 17, wherein the non-transactional mode is a mode in which the slave processors are in a spin loop without generating any external bus transactions.

22. The computer program product of claim 17, wherein the third instructions comprises:

sub-instructions for setting a register in the system core logic to a value for the another frequency.

23. A data processing system comprising:

a bus system;

a memory connected to the bus system, wherein the memory includes a set of instructions; and

a processing unit connected to the bus system, wherein the processing unit executes a set of instructions to determine whether the operating frequency should be changed from the default frequency to the another frequency; place slave processors in the multi-processor data processing system into a non-transactional mode in response to determining the operating frequency

should be changed from a default frequency to another frequency; and change the operating frequency in the system core logic to the another frequency.